UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/548,313	04/12/2000	Hidehiko Kira	000452	6169

23850 7590 03/28/2002

ARMSTRONG,WESTERMAN & HATTORI, LLP
1725 K STREET, NW.
SUITE 1000
WASHINGTON, DC 20006

EXAMINER	
RENNER, CRAIG A	
ART UNIT	**PAPER NUMBER**
2652	

DATE MAILED: 03/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	Application No. 09/548,313	Applicant(s) Kira et al.
	Examiner Craig A. Renner	Art Unit 2652

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *14 Mar 2002*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above, claim(s) *10-29* is/are withdrawn from consideration.

5) ☐ Claim(s) ______ is/are allowed.

6) ☒ Claim(s) *1-9* is/are rejected.

7) ☐ Claim(s) ______ is/are objected to.

8) ☐ Claims ______ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on ______ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on ______ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ______.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 2 & 4

18) ☐ Interview Summary (PTO-413) Paper No(s). ______

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

Election/Restriction

1. Claims 14-29 are withdrawn from further consideration pursuant to 37 C.F.R. § 1.142(b) as being drawn to non-elected inventions, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 7, filed 4 February 2002.

2. Applicant's election without traverse of "Group (I), Claims 1-9" in Paper No. 9, filed 14 March 2002, is acknowledged. Accordingly, claims 10-13 are withdrawn from further consideration pursuant to 37 C.F.R. § 1.142(b) as being drawn to a non-elected invention, there being no allowable generic or linking claim.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. § 119(a)-(d), which papers have been placed of record in the file.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 U.S.C. § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

7. Claims 1-2, 5 and 8 are rejected under 35 U.S.C. § 102(e) as being anticipated by Shiraishi (US 6,282,062).

With respect to claims 1-2 and 5, Shiraishi teaches a head assembly (10) comprising a mounting surface (11); and an integrated circuit chip (13) which is mounted on the mounting surface and processes signals, the integrated circuit chip being covered by a layer (25) [as per claim 1]; wherein the layer covering the integrated circuit chip is formed (as shown in Fig. 3, for instance) [as per claim 2]; wherein the layer covers at least peripheral portions of the integrated circuit chip (as shown in Fig. 3, for instance) [as per claim 5]. As the claims are directed to head assembly, per se, the method limitation(s) appearing in line 3 of claim 2 can only be accorded

weight to the extent that it/they affects the structure of the completed head assembly. Note that "[d]etermination of patentability in 'product-by-process' claims is based on product itself, even though such claims are limited and defined by process [i.e., "evaporation"], and thus product in such claim is unpatentable if it is the same as, or obvious form, product of prior art, even if prior product was made by a different process", *In re Thorpe, et al.*, 227 USPQ 964 (CAFC 1985). Furthermore, note that a "[p]roduct-by-process claim, although reciting subject matter of claim in terms of how it is made [i.e.,"evaporation"], is still product claim; it is patentability of product claimed and not recited process steps that must be established, in spite of fact that claim may recite only process limitations", *In re Hirao and Sato*, 190 USPQ 685 (CCPA 1976).

With respect to claim 8, Shiraishi teaches a disk unit (lines 12-17 in column 1, for instance) for reading information from and writing information to a disk (line 15 in column 1, for instance), comprising a head assembly (10) having a mounting surface (11), a head (12) mounted on the mounting surface, and an integrated circuit chip (13) which is mounted on the mounting surface and processes information read from and/or written to the disk via the head, the integrated circuit chip being covered by a layer (25) [as per claim 8].

Claim Rejections - 35 U.S.C. § 103

8. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

> such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103(a).

10. Claims 3, 6 and 9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shiraishi (US 6,282,062).

Shiraishi teaches the disk unit/head assembly as detailed in paragraph 7, supra, further wherein the layer covers at least peripheral portions of the integrated circuit chip (as shown in Fig. 3, for instance) [as per claim 9]. Shiraishi, however, remains silent as to the layer being made of "poly(p-xylylene)" [as per claim 3], and the layer being made of a "low-viscosity resin selected from a group consisting of photo-curing resins including ultraviolet-curing resins, and thermosetting resins" [as per claims 6 and 9].

Official notice is taken of the fact that poly(p-xylylene) is a notoriously old and well known chip covering layer material. Official notice is also taken of the fact that a low-viscosity resin selected from a group consisting of photo-curing resins including ultraviolet-curing resins, and thermosetting resins is a notoriously old and well known chip covering layer material. It

would have been obvious to a person having ordinary skill in the art at the time the invention was made to have had the layer of Shiraishi be made of poly(p-xylylene) [as per claim 3], and/or the layer of Shiraishi be made of a low-viscosity resin selected from a group consisting of photo-curing resins including ultraviolet-curing resins, and thermosetting resins [as per claims 6 and 9]. The rationale is as follows:

One of ordinary skill in the art would have been motivated to have had have had the layer of Shiraishi be made of poly(p-xylylene) [as per claim 3], and/or the layer of Shiraishi be made of a low-viscosity resin selected from a group consisting of photo-curing resins including ultraviolet-curing resins, and thermosetting resins [as per claims 6 and 9] since each is a notoriously old and well known chip covering layer material, and since selecting a known material on the basis of its suitability for the intended use is within the level of ordinary skill in the art, *In re Leshin*, 125 USPQ 416 (CCPA 1960).

11. Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Shiraishi (US 6,282,062) in view of Japanese Laid-Open Utility Model Application (JP 57-057556).

Shiraishi teaches the head assembly as detailed in paragraph 7, supra, further wherein the integrated circuit chip has a first surface provided with conductor bumps (each 28), and a second surface opposite to the first surface (as shown in Fig. 3, for instance). Shiraishi, however, remains silent as to the peripheral portion of the second surface being "chamfered."

Japanese Laid-Open Utility Model Application (JP 57-057556) teaches a peripheral portion of a non-mounting surface of an integrated circuit chip being chamfered for the purpose of facilitating handling while reducing damage potential. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have had the peripheral portion of the second surface of Shiraishi be chamfered as taught by Japanese Laid-Open Utility Model Application (JP 57-057556). The rationale is as follows:

One of ordinary skill in the art would have been motivated to have had have had the peripheral portion of the second surface of Shiraishi be chamfered as taught by Japanese Laid-Open Utility Model Application (JP 57-057556) since such facilitates handling while reducing damage potential.

12. Claim 7 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Shiraishi (US 6,282,062) in view of Shiraishi et al. (US 6,084,746).

Shiraishi (US 6,282,062) teaches the head assembly as detailed in paragraph 7, supra, further wherein the head assembly further comprises a head slider (12) provided with a head (line 17 in column 3, for instance). Shiraishi (US 6,282,062), however, remains silent as to the integrated circuit chip height being "lower than a height of the head slider from the mounting surface."

Shiraishi et al. (US 6,084,746) teaches a height (H1) of an integrated circuit chip (20) being lower than a height (H2) of a head slider (19) from a mounting surface (31) in the same

field of endeavor for the purpose of avoiding disk interference therewith. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have had the integrated circuit chip height of Shiraishi (US 6,282,062) be lower than a height of the head slider from the mounting surface as taught by Shiraishi et al. (US 6,084,746). The rationale is as follows:

One of ordinary skill in the art would have been motivated to have had the integrated circuit chip height of Shiraishi (US 6,282,062) be lower than a height of the head slider from the mounting surface as taught by Shiraishi et al. (US 6,084,746) since such avoids disk interference therewith.

Pertinent Prior Art

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. This includes Yasuda et al. (JP 61-104313), Namikata (JP 04-047511) and Hirai et al. (JP 10-293915) , which each individually teaches a head assembly with an integrated circuit chip covered by a layer.

Conclusion

14. Any inquiry concerning the above referenced application should be directed to the examiner, Craig A. Renner, whose telephone number is (703) 308-0559, and whose facsimile

number is (703) 872-9314. The examiner can normally be reached Tuesday through Friday from 7:30 a.m. to 6:00 p.m. E.S.T.

Craig A. Renner
Primary Examiner
Art Unit 2652

CAR
March 24, 2002